

30V P-Channel Enhancement Mode MOSFET

Description

The PECN3007DR uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

General Features

- ◆ $V_{DS} = -30V$, $I_D = -7A$
 $R_{DS(ON)}(Typ.) = 36m\Omega$ @ $V_{GS} = -4.5V$
 $R_{DS(ON)}(Typ.) = 28m\Omega$ @ $V_{GS} = -10V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

Application

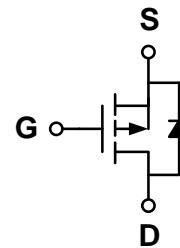
- ◆ PWM applications
- ◆ Load switch

Package

- ◆ DFN2*2-6L-B

100% UIS TESTED!
100% ΔV_{ds} TESTED!

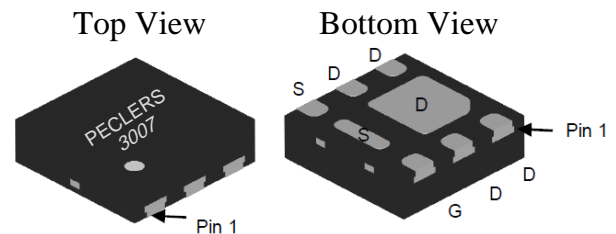
Schematic diagram



Marking and pin assignment

DFN2*2-6L-B

(Thickness 0.55mm)



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN3007DR	-55°C to +150°C	DFN2*2-6L-B	4000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	± 20	V
Drain current-continuous ^a @ $T_j = 125^\circ C$ -pulse ^b	I_D	-7	A
	I_{DM}	-28	A
Drain-source Diode forward current	I_S	-7	A
Maximum power dissipation	P_D	18	W
Operating junction Temperature range	T_j	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8	-1.3	-2	V
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-7A$	-	28	35	m Ω
		$V_{GS}=-4.5V, I_D=-5A$	-	36	45	
Forward transconductance	gfs	$V_{GS}=-5V, I_D=-7A$	-	5	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	$V_{DS}=-15V, V_{GS}=0V$ $f=1.0MHz$	-	760	-	pF
Output capacitance	C_{OSS}		-	140	-	
Reverse transfer capacitance	C_{RSS}		-	95	-	
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	$V_{DS}=-15V$ $V_{GS}=-10V$ $R_L=2.3\Omega$ $R_{GEN}=3\Omega$	-	8	-	ns
Rise time	t_r		-	6	-	
Turn-off delay time	$t_{D(OFF)}$		-	17	-	
Fall time	t_f		-	5	-	
Total gate charge	Qg	$V_{DS}=-15V, I_D=-6A$ $V_{GS}=-10V$	-	13.6	-	nC
Gate-source charge	Qgs		-	2.5	-	
Gate-drain charge	Qgd		-	3.2	-	
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_S=-1.25A$	-	-0.81	-1.2	V

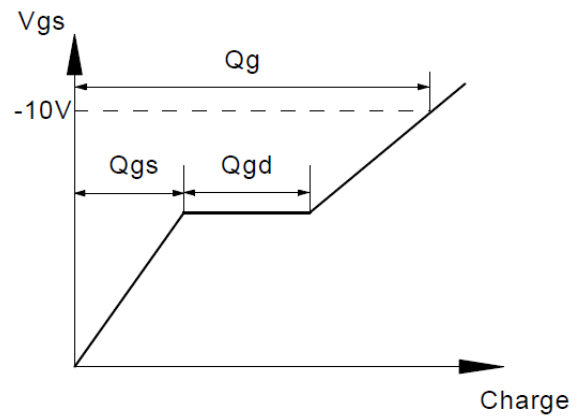
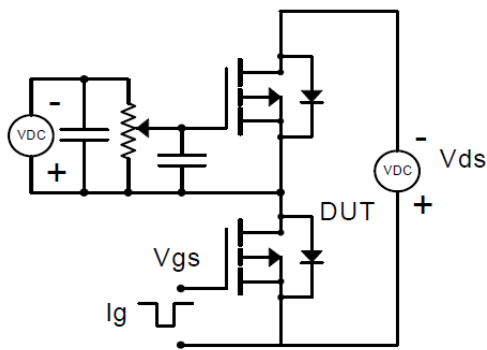
Notes:

- surface mounted on FR4 board, $t \leq 10sec$
- pulse test: pulse width $\leq 300\mu s$, duty $\leq 2\%$
- guaranteed by design, not subject to production testing

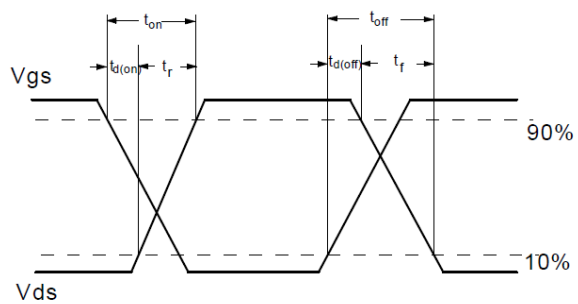
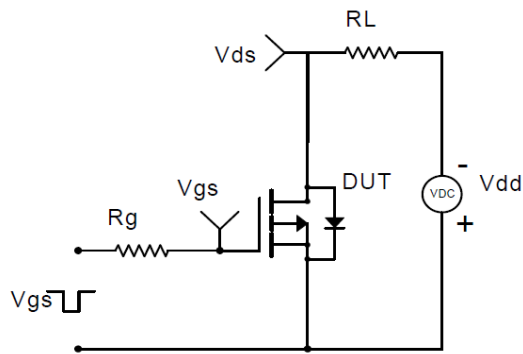
Thermal Characteristics

Thermal Resistance junction-to ambient	Rth JA	100	°C/W
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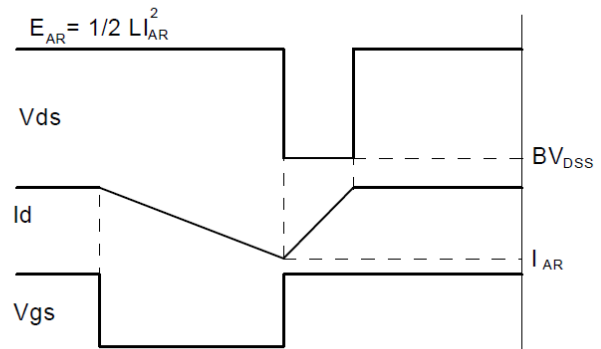
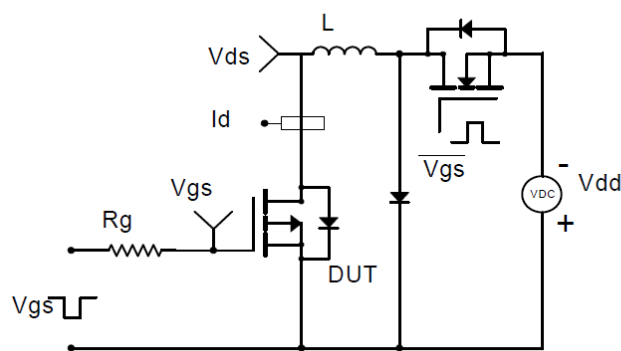
Gate Charge Test Circuit & Waveform



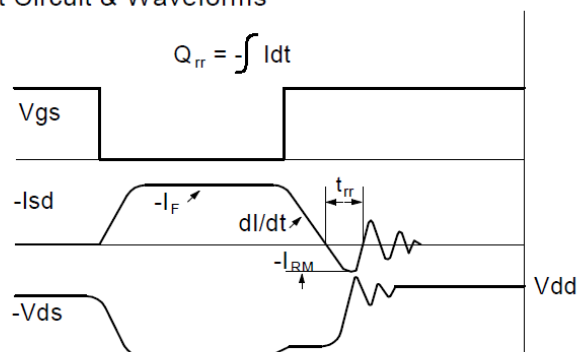
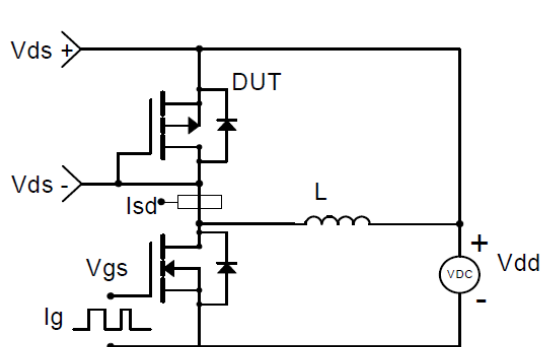
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

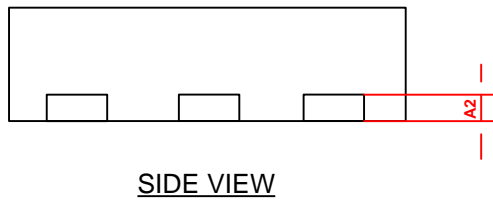


Diode Recovery Test Circuit & Waveforms

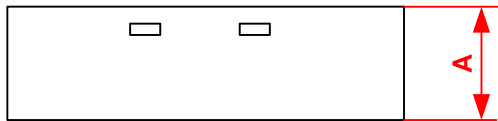


Package Information

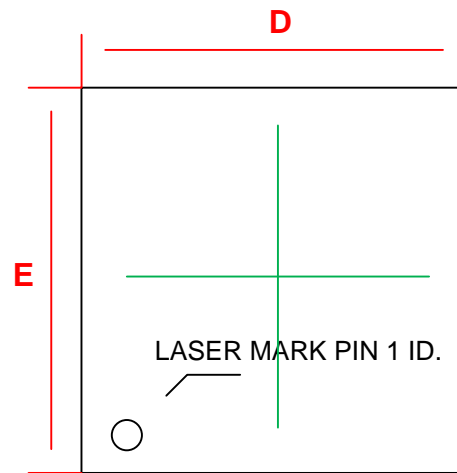
- DFN2*2-6L-B



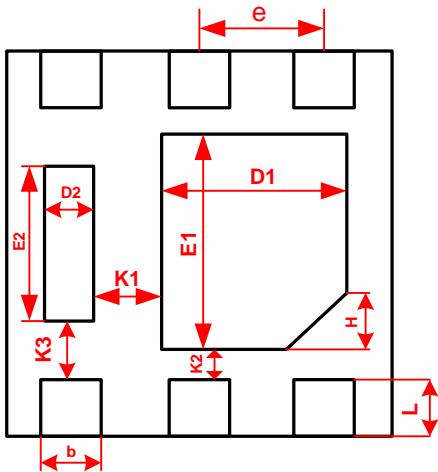
SIDE VIEW



SIDE VIEW



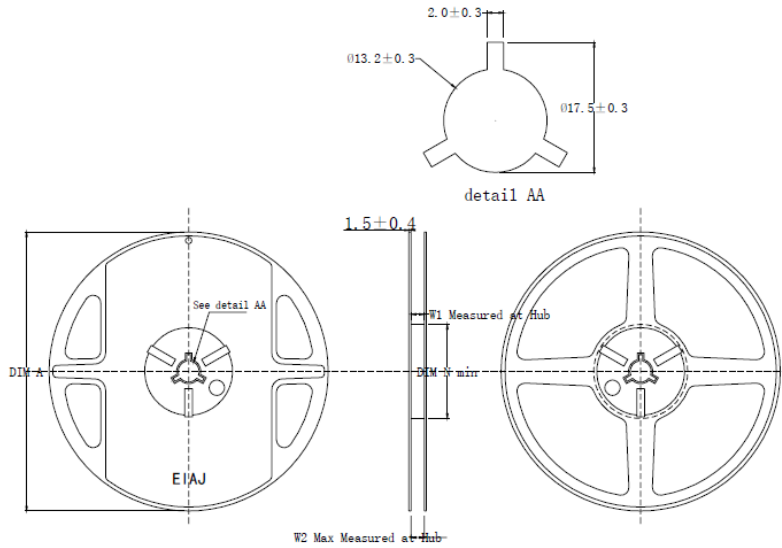
TOP VIEW



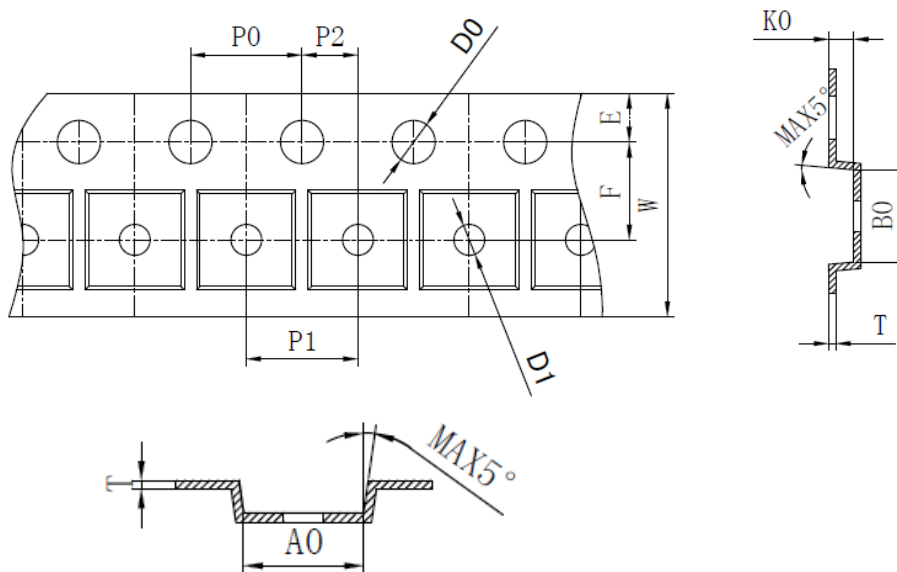
BOTTOM VIEW

Common Dimension (mm)			
PKG	DFN2020-6L-B		
SYMBOL	MIN.	MON.	MAX.
A	0.527	0.552	0.577
A2		0.127REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.85	0.95	1.05
E1	1.05	1.15	1.25
D2	0.20	0.25	0.30
E2	0.69	0.79	0.89
e	0.55	0.65	0.75
H	0.25	0.30	0.35
K1	0.25MIN		
K2	0.15MIN		
K3	0.20MIN		
L	0.20	0.25	0.30

Tape and Reel



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ϕA	ϕN	W1 (Min)	W2 (Max)
8MM	178 ± 2.0	60 ± 1.0	8.4	11.4
12MM	178 ± 2.0	60 ± 1.0	12.4	15.4



SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	2.20 ± 0.05	2.20 ± 0.05	0.75 ± 0.10	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.20 ± 0.03	1.75 ± 0.10	3.50 ± 0.05	1.55 ± 0.05	$1.00^{+0.10}_{-0}$	$8.00^{+0.20}_{-0.10}$