30V N-Channel Enhancement Mode MOSFET

Description

The PECN3400VR-S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and high density cell Design for ultra low on-resistance. This device is suitable for use as a load switch or in PWM applications.

General Features

- V_{DS} =30V，I_D =5.8A
  $R_{DS(ON)}$(Typ.)=26mΩ @V_{GS}=4.5V
  $R_{DS(ON)}$(Typ.)=33mΩ @V_{GS}=2.5V
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

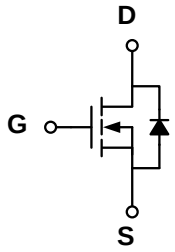
Application

- PWM applications
- Load switch

Package

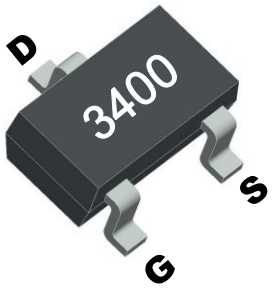
- SOT-23

Schematic diagram



Marking and pin assignment

SOT-23
(TOP VIEW)



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN3400VR--S-G	-55°C to +150°C	SOT-23	3000

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	±12	V
Continuous Drain Current	25°C	I_D	5.8	A
	100°C		5	
Plused Drain Current		I_{DM}	28	A
Avalanche energy[A]		E_{AS}	18	mJ
Power Dissipation[B]	25°C	P_D	1.4	W
	100°C		0.6	
Operating junction Temperature range		Tj	-55-150	℃

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	μA
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	0.5	0.8	1.3	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=6A	-	26	30	mΩ
		V_{GS}=2.5V, I_D=5A	-	33	35	
Forward Transconductance	g_{FS}	V_{DS}=15V,I_D=6A	-	33	-	S
Diode Characteristics						
Diode Forward Voltage	V_{SD}	I_{SD}= 2A,V_{GS}=0V	-	0.7	1	V
Diode Continuous Forward Current	I_S		-	-	6	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S, di/dt = 100A/μs	-	8.5	-	ns
Reverse Recovery Charge	Q_{rr}		-	2.6	-	nC
Dynamic Characteristics						
Gate Resistance	R_G	V_{GS}=0V, V_{DS}=0V,f=1MHz	-	-	5	Ω
Input capacitance	C_{ISS}	V_{GS}=0V ,V_{DS}=15V f=1.0MHz	-	519	-	pF
Output capacitance	C_{OSS}		-	45	-	
Reverse transfer capacitance	C_{RSS}		-	38	-	
Turn-on delay time	$t_{D(ON)}$	V_{GS}=5V, V_{DS}=15V, R_L=1.5Ω, R_G=3Ω	-	3	-	ns
Turn-on Rise time	tr		-	2.5	-	
Turn-off delay time	$t_{D(OFF)}$		-	25	-	
Turn-off Fall time	t_f		-	4	-	
Total gate charge	Q_g	V_{GS}=5V, V_{DS}=15V， I_D=6A	-	11	-	nC
Gate-source charge	Q_{gs}		-	1	-	
Gate-drain charge	Q_{gd}		-	1.2	-	

Thermal Characteristics

Thermal Resistance,Junctuion-to-Ambient[B]	$R_{\theta JA}$	90	℃/W

A. E_{AS} Condition: (T_j=25℃ ,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω)

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Surface Mounted on FR4 Board, t ≤ 10 sec.

Typical Performance Characteristics

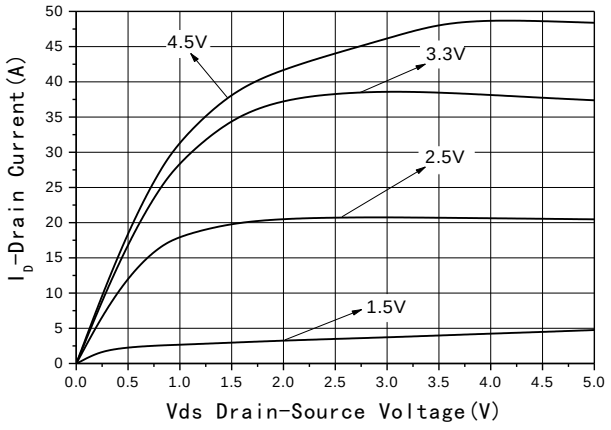


Fig1 Output Characteristics

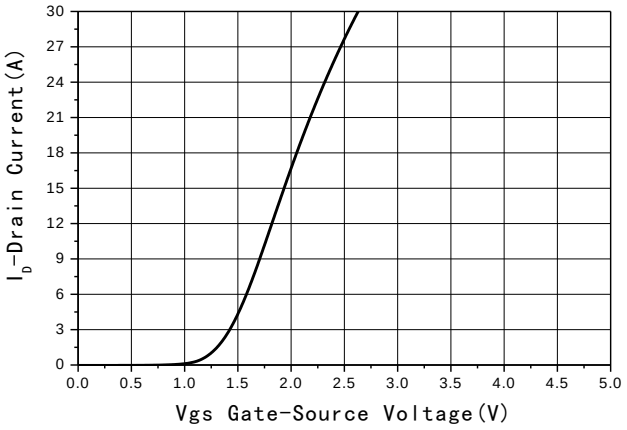


Fig2 Transfer Characteristics

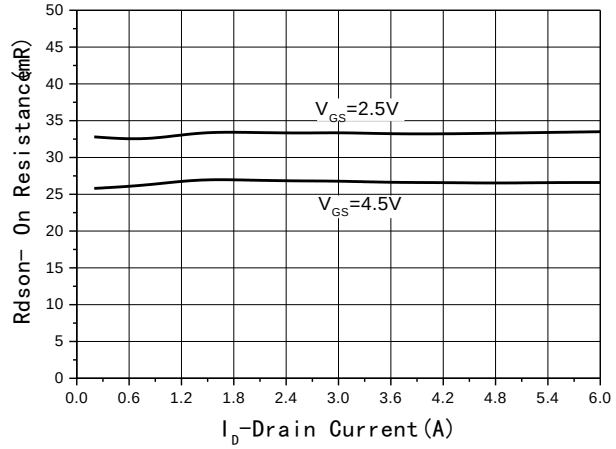


Fig3 Rdson-Drain current

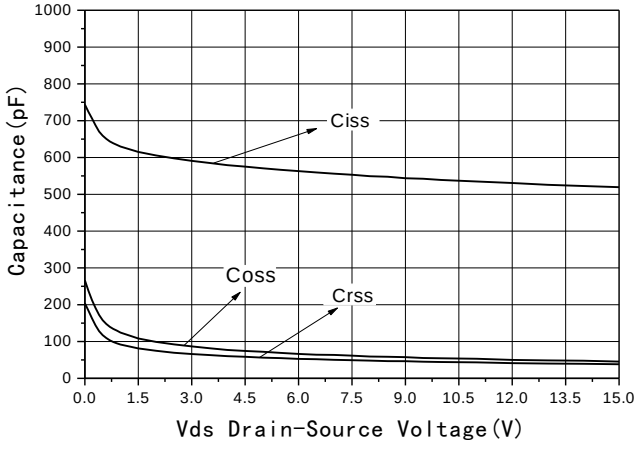


Fig4 Capacitance vs Vds

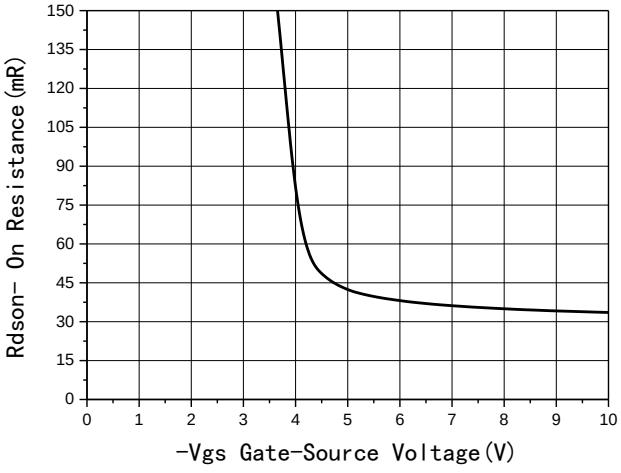


Fig5 Rdson-Gate Drain voltage

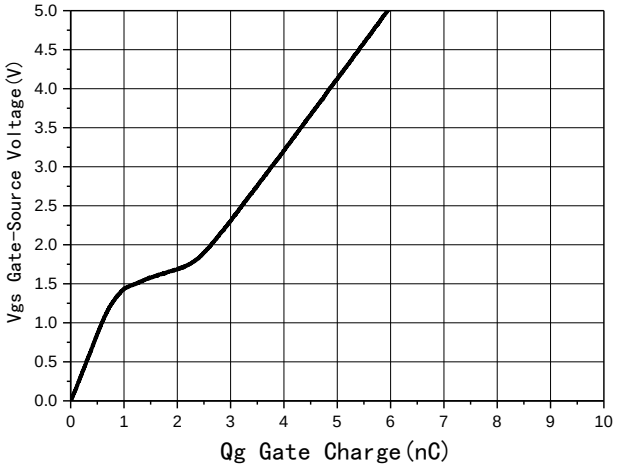


Fig6 Gate Charge

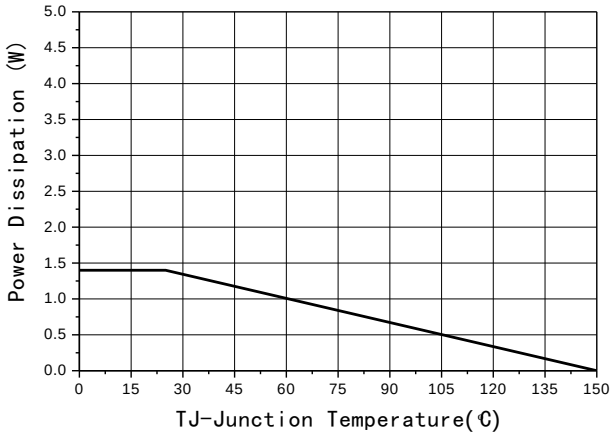


Fig7 Power De-rating

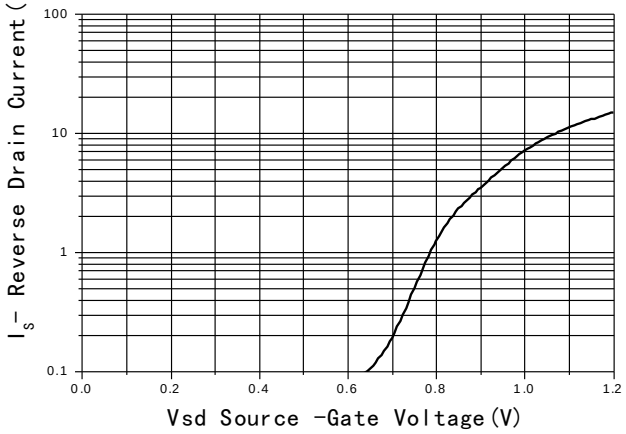


Fig8 Source-Drain Diode Forward

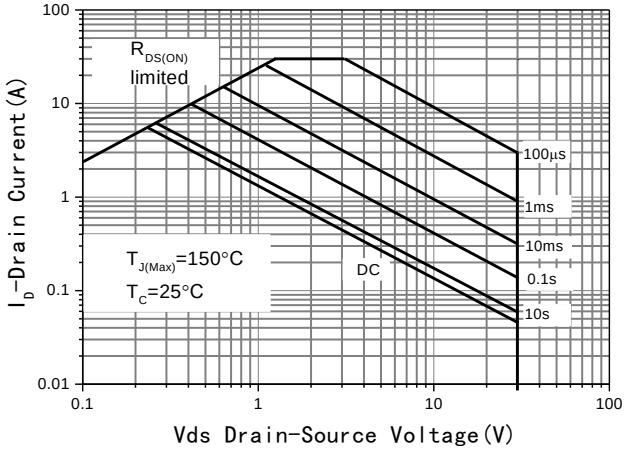


Fig9 Safe Operating Area

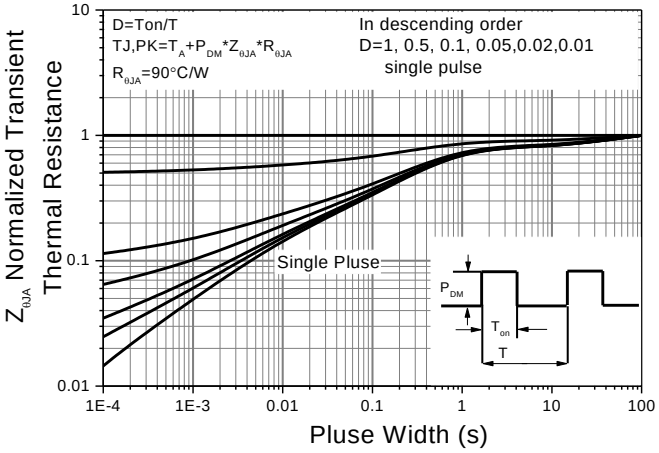
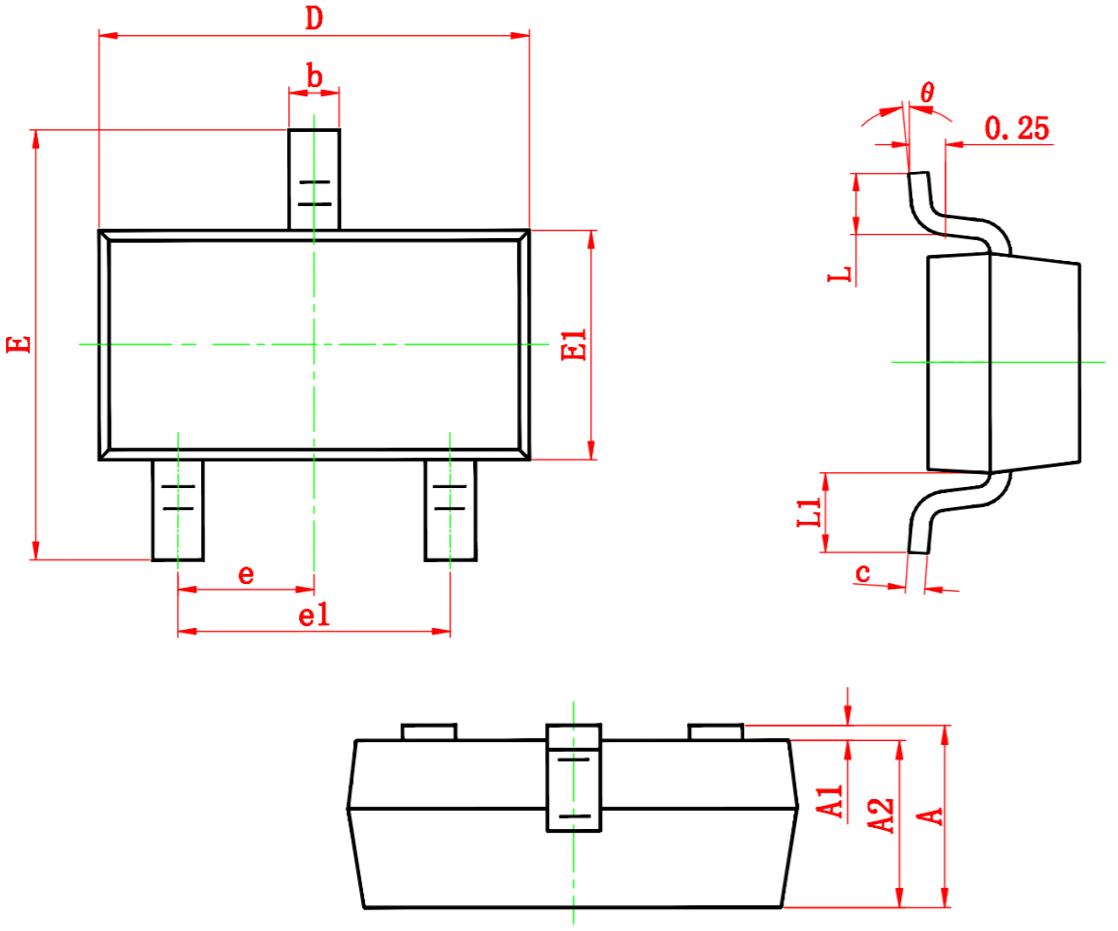


Fig10 Transient Thermal Response Curve

Package Information

- **SOT-23**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	2.250	2.550	0.089	0.100
E1	1.200	1.400	0.047	0.055
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.300	0.500	0.012	0.020
L1	0.550 REF.		0.022 REF.	
θ	0°	8°	0°	8°