

20V N-Channel Enhancement Mode MOSFET

Description

The PECN3416E uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

General Features

- ◆ $V_{DS} = 20V$, $I_D = 7A$
 $R_{DS(ON)}(Typ.) = 17.5m\Omega$ @ $V_{GS} = 2.5V$
 $R_{DS(ON)}(Typ.) = 14.5m\Omega$ @ $V_{GS} = 4.5V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package
- ◆ ESD Rating: 3500V HBM

Application

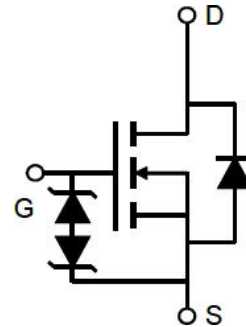
- ◆ PWM applications
- ◆ Load switch

Package

- ◆ SOT-23-3L

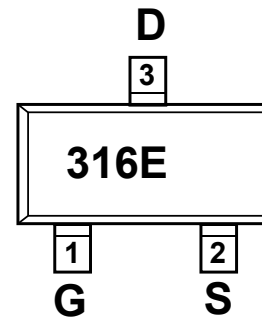


Schematic diagram



Marking and pin assignment

SOT-23-3L
(TOP VIEW)



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN3416EM R-G	-55°C to +150°C	SOT-23-3L	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	±8	V
Drain current-continuous ^a @Tj=125°C -pulse ^d		I_D	7	A
		I_{DM}	28	A
Maximum power dissipation	T _A =25°C	P _D	1.4	W
	T _A =70°C		0.9	
Operating junction Temperature range		T _j	-55—150	°C

Notes:

- a. surface mounted on FR4 board, t_s≤10sec
- b. pulse test: pulse width≤300μs, duty≤2%

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	-1	μA
Gate-body leakage	I _{GSS}	V _{DS} =0V, V _{GS} =±8V	-	-	±1	μA
		V _{DS} =0V, V _{GS} =±10V			±3	
		V _{DS} =0V, V _{GS} =±12V			±10	
ON Characteristics						
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45	0.62	1.00	V
Drain-source on-state resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =7A	-	14.5	18	mΩ
		V _{GS} =2.5V, I _D =4A	-	17.5	22	
		V _{GS} =1.8V, I _D =3A	-	27.0	39	
Forward transconductance	g _{fs}	V _{GS} =5V, I _D =7A	-	50	-	S
Dynamic Characteristics						
IPECNut capacitance	C _{ISS}	V _{DS} =10V ,V _{GS} =0V f=1.0MHz	-	1300	-	pF
Output capacitance	C _{OSS}		-	165	-	
Reverse transfer capacitance	C _{RSS}		-	90	-	
Switching Characteristics						
Turn-on delay time	t _{D(ON)}	V _{DD} =10V V _{GS} =4.5V R _L =1.54ohm R _{GEN} =3ohm	-	290	-	ns
Rise time	tr		-	330	-	
Turn-off delay time	t _{D(OFF)}		-	3.8	-	
Fall time	tf		-	2.4	-	
Total gate charge	Qg	V _{DS} =10V,I _D =7A V _{GS} =4.5V	-	10.5	-	nC
Gate-source charge	Qgs		-	4.3	-	
Gate-drain charge	Qgd		-	2.7	-	
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode forward voltage	V _{SD}	V _{GS} =0V,I _s =4A	-	-0.82	-1.2	V

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient ^A	$\leq 10s$	$R_{\theta JA}$	70	°C/W
Maximum Junction-to-Ambient ^A	Steady-State		100	
Maximum Junction-to-Lead ^B	Steady-State	$R_{\theta JL}$	63	

c. A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ C$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10s$ thermal resistance rating.

d. B: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

Typical Performance Characteristics

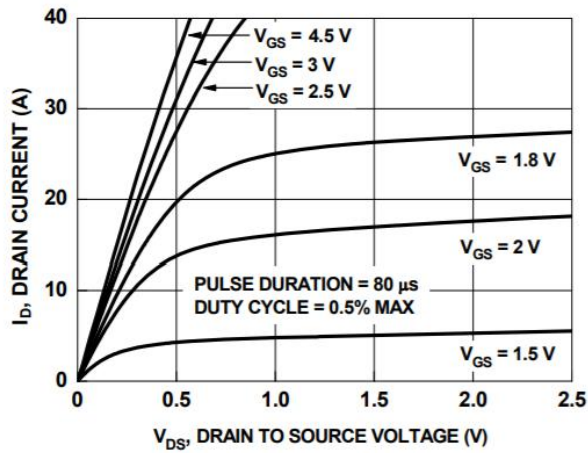


Figure 1. On Region Characteristics

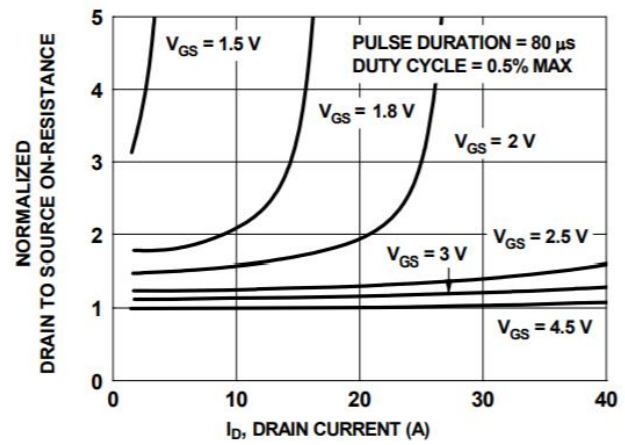


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

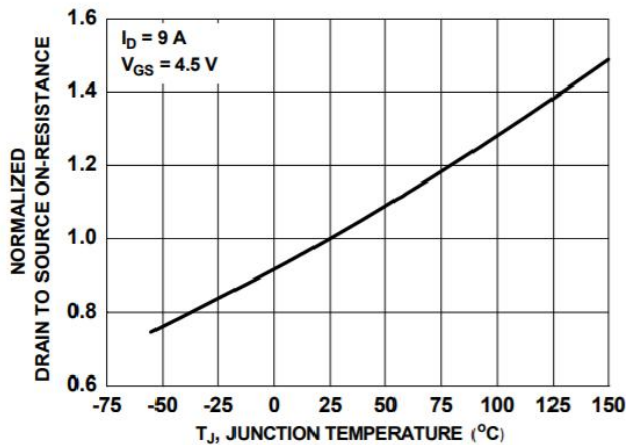


Figure 3. Normalized On Resistance vs Junction Temperature

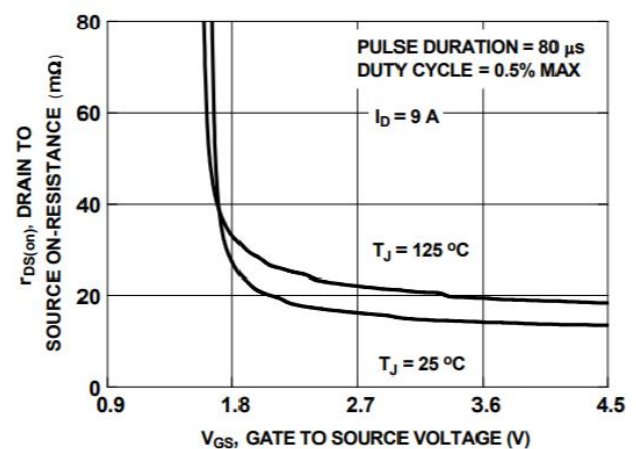


Figure 4. On-Resistance vs Gate to Source Voltage

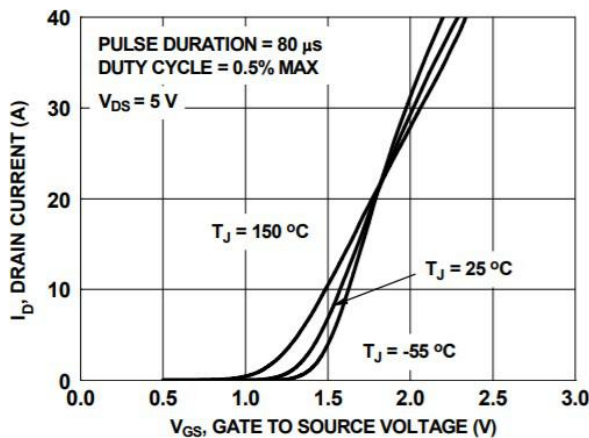


Figure 5. Transfer Characteristics

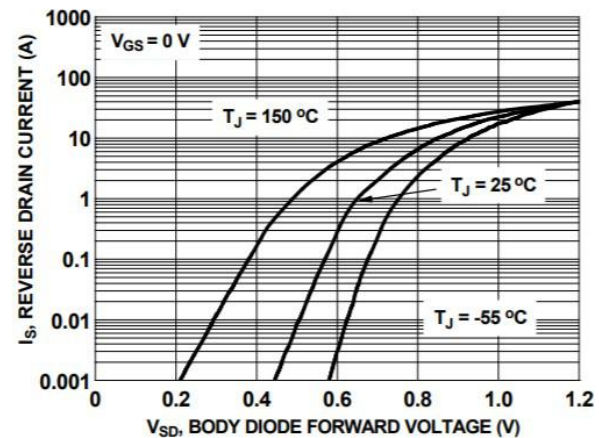


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

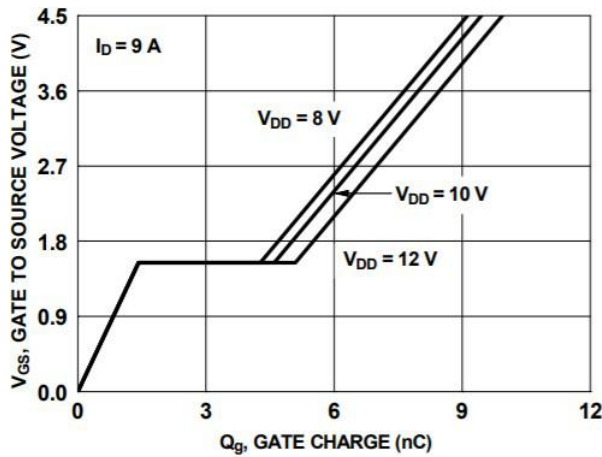


Figure 7. Gate Charge Characteristics

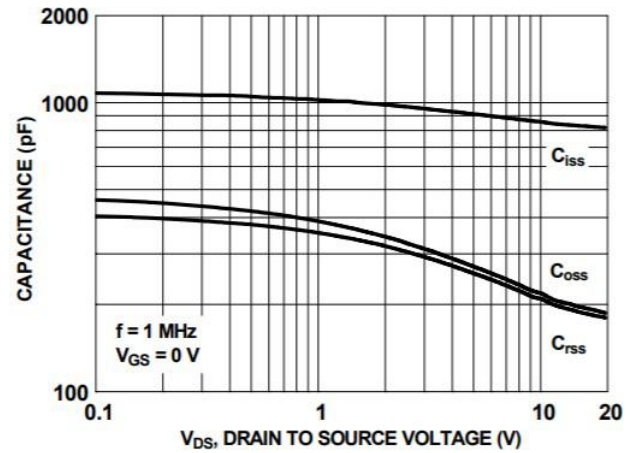


Figure 8. Capacitance vs Drain to Source Voltage

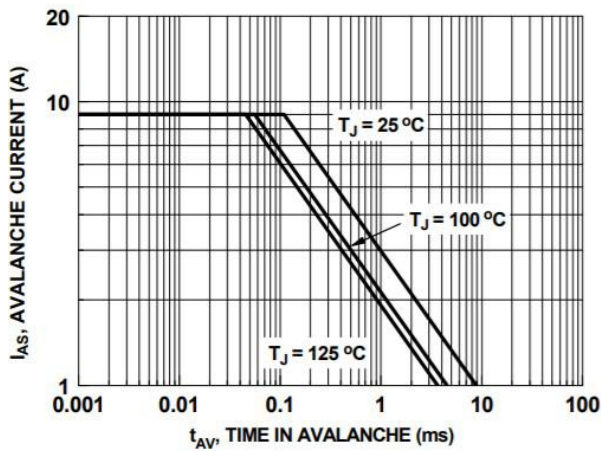


Figure 9. Unclamped Inductive Switching Capability

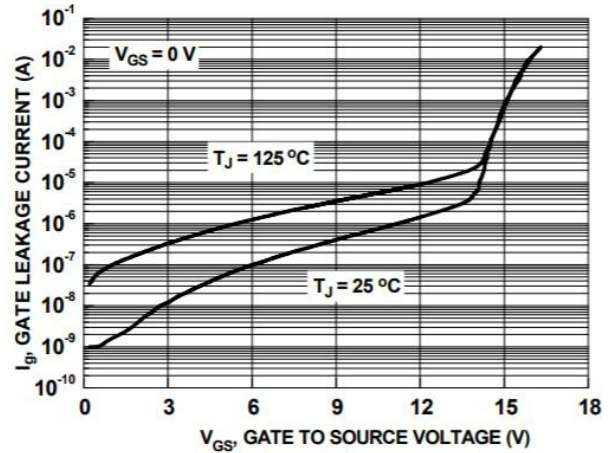


Figure 10. Gate Leakage Current vs Gate to Source Voltage

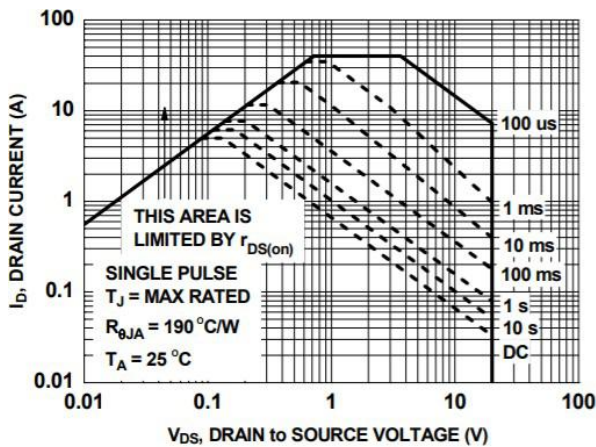


Figure 11. Forward Bias Safe Operating Area

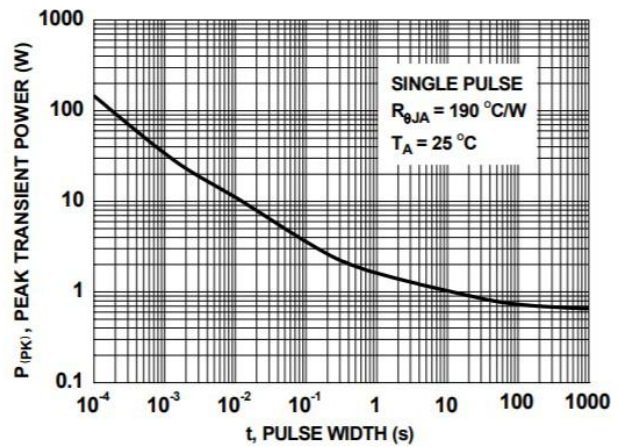
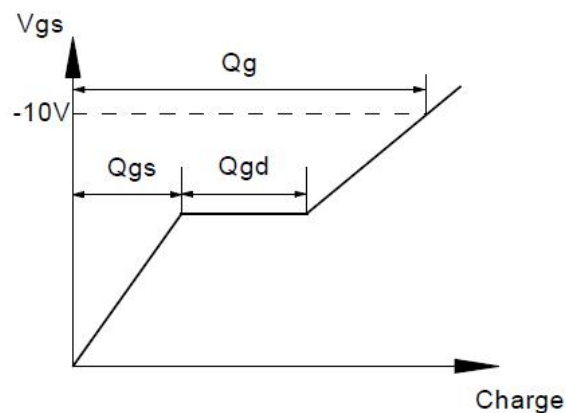
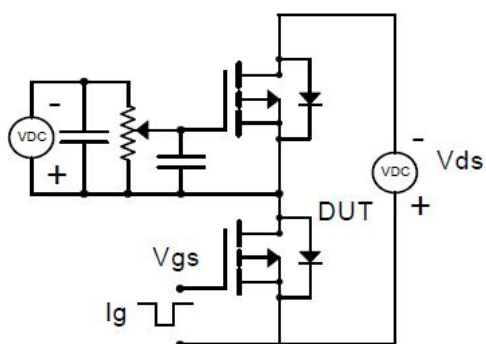
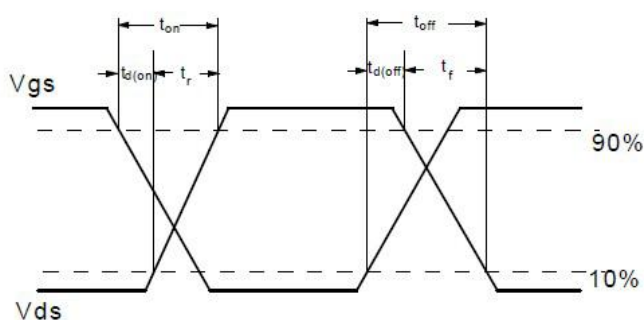
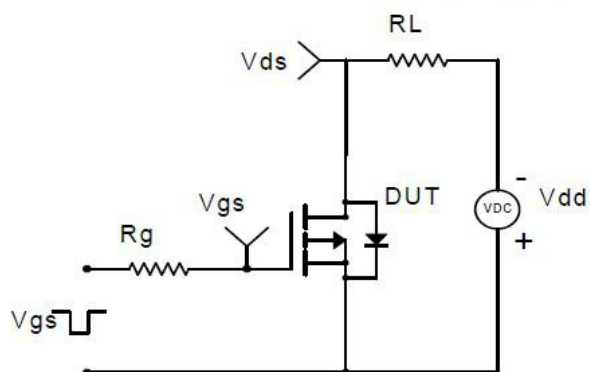


Figure 12. Single Pulse Maximum Power Dissipation

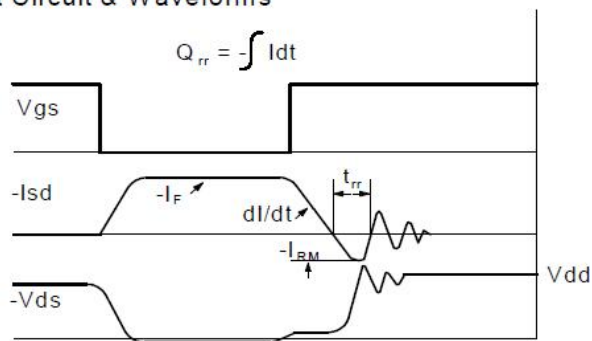
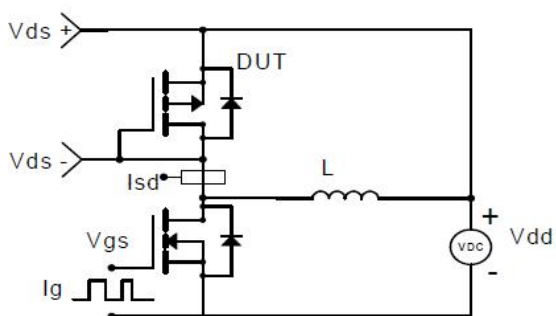
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

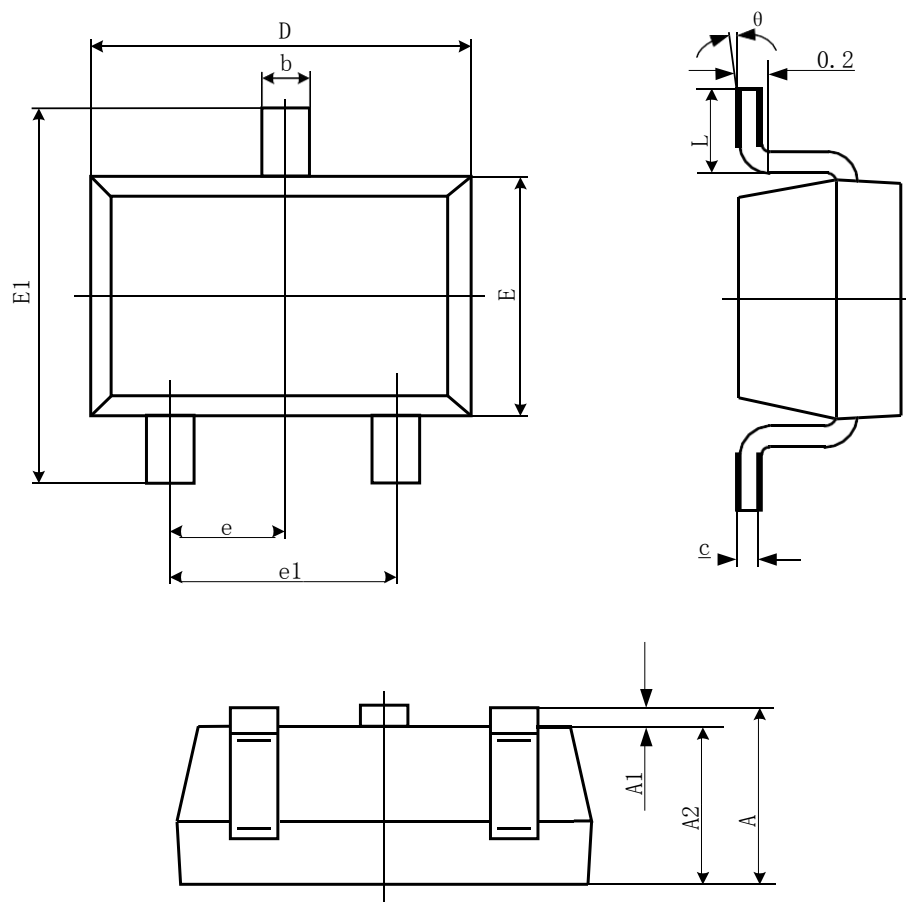


Diode Recovery Test Circuit & Waveforms



Package Information

- SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°