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PECN4840SR

40V Dual N-Channel Enhancement Mode MOSFET

Description

The PECN4840SR uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge.This device is suitable for high side switch in SMPS and general purpose applications.

General Features

◆ V_{DS} =40V，ID =6A

$R_{DS(ON)}$=27mΩ (typical) @ VGS=10V

$R_{DS(ON)}$=34mΩ (typical) @ VGS=4.5V

◆ Excellent gate charge x $R_{DS(ON)}$ product(FOM)
◆ Very low on-resistance $R_{DS(ON)}$
◆ 150 °C operating temperature
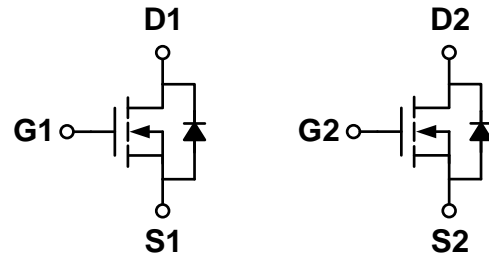◆ Pb-free lead plating
◆ 100% UIS tested

Application

◆ DC/DC Converter
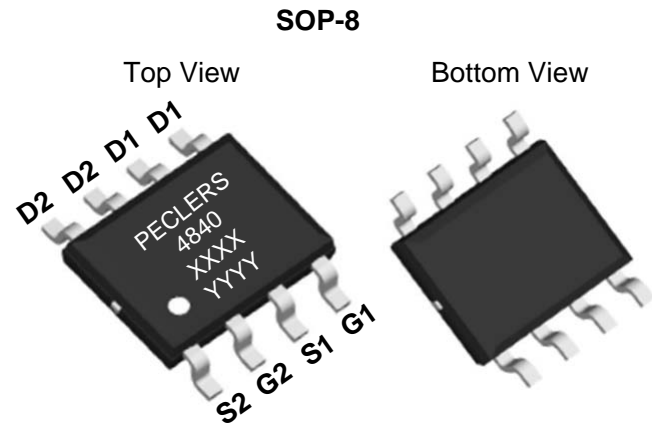◆ Ideal for high-frequency switching and synchronous rectification

Package

◆ SOP-8

Schematic diagram

Marking and pin assignment

SOP-8

Top View   Bottom View

XXXX—Wafer Information

YYYY—Quality Code

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN4840SR	-55°C to +150°C	SOP-8	4000

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	±20	V
Drain Current-Continuous (Silicon Limited)	T_A=25°C	I_D	6	A
	T_A=75°C		5	
Pulsed Drain Current (Package Limited)		I_{DM}	24	A
Single pulse avalanche energy		E_{AS}	10	mJ
Maximum power dissipation	T_A=25°C	P_D	2	W
	T_A=75°C		1.3	

| Operating junction Temperature range | | | Tj | -55—150 | ℃ |

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250µA	40	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	µA
Gate-body leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250µA	1.0	1.45	2	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A	-	27	30	mΩ
		V_{GS}=4.5V, I_D=5A	-	34	38	
Forward transconductance	gfs	V_{DS}=5V, I_D=6A	-	27	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	V_{DS}=20V ,V_{GS}=0V f=1.0MHz	-	549	-	pF
Output capacitance	C_{OSS}		-	87	-	
Reverse transfer capacitance	C_{RSS}		-	54	-	
Gate resistance	Rg	V_{GS}=0V, V_{DS}=0V, f=1.0MHz	-	4.5	7	Ω
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	V_{DS}=20V V_{GS}=10V R_L=1.5Ω R_{GEN}=3Ω	-	6.4	-	ns
Rise time	tr		-	3.6	-	
Turn-off delay time	$t_{D(OFF)}$		-	16.2	-	
Fall time	tf		-	6.5	-	
Total gate charge	Qg	V_{DS}=20V,I_D=6A V_{GS}=10V	-	4.75	-	nC
Gate-source charge	Qgs		-	1.9	-	
Gate-drain charge	Qgd		-	1.08	-	

Thermal Characteristics

Parameter		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient[A]	≤ 10s	$R_{θJA}$	33	40	℃/W
Maximum Junction-to-Ambient[A]	Steady-State		59	75	
Maximum Junction-to-Lead[B]	Steady-State	$R_{θJC}$	16	24	

A:The value of R qJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: The R qJA is the sum of the thermal impedence from junction to lead R qJL and lead to ambient.

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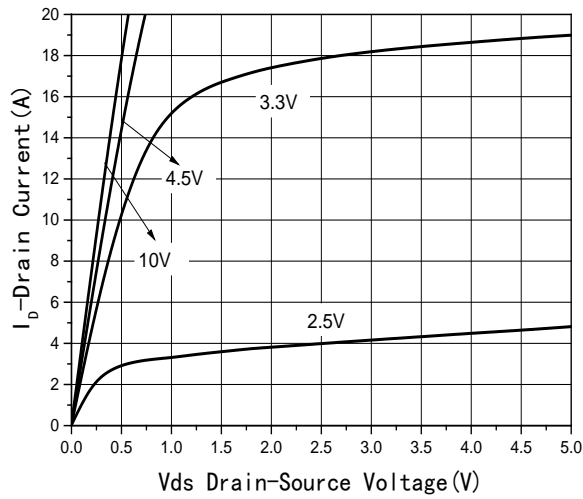## Typical Performance Characteristics

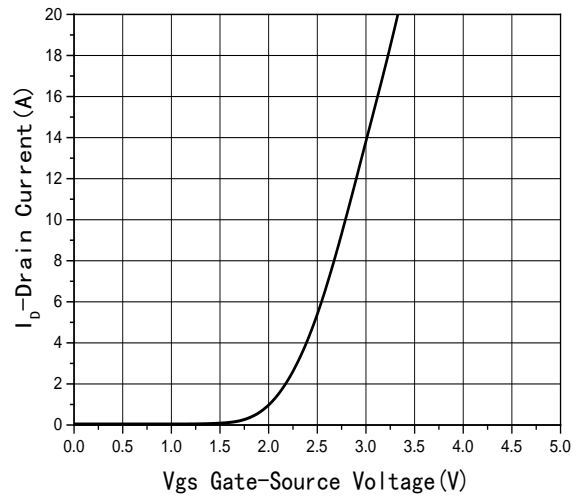**Fig1 Output Characteristics**
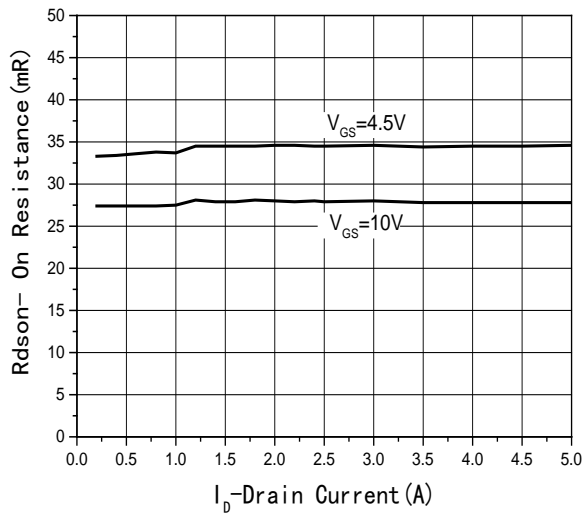

Fig2 Transfer Characteristics
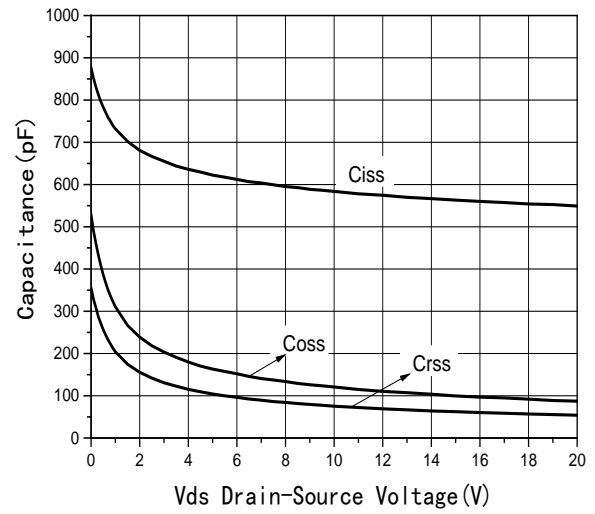

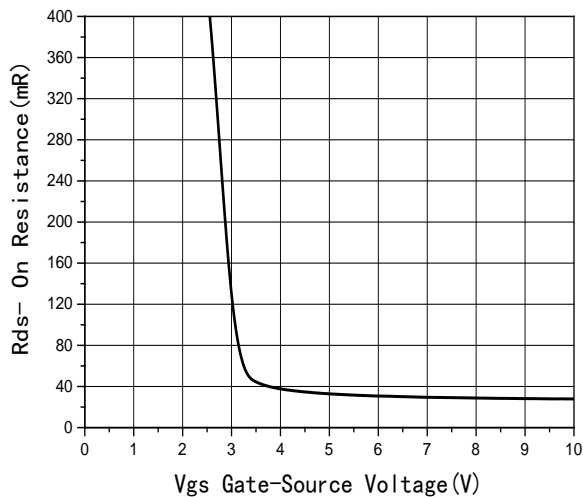**Fig3 Rdson-Drain current**

Fig4 Capacitance vs Vds
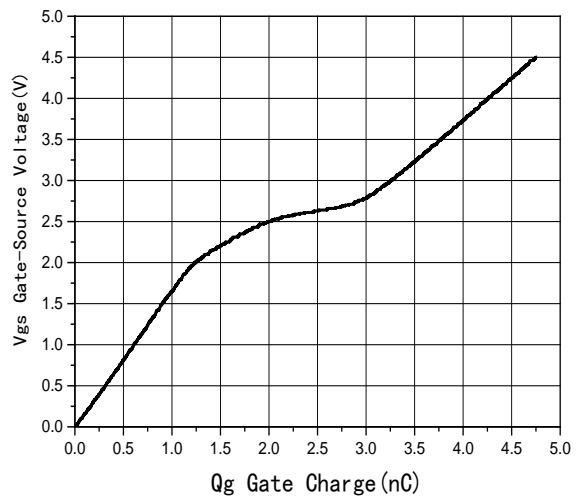
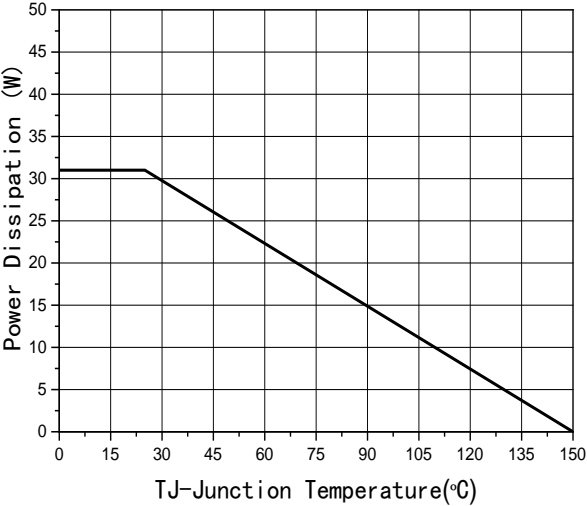

Fig5 Rdson-Gate Drain voltage
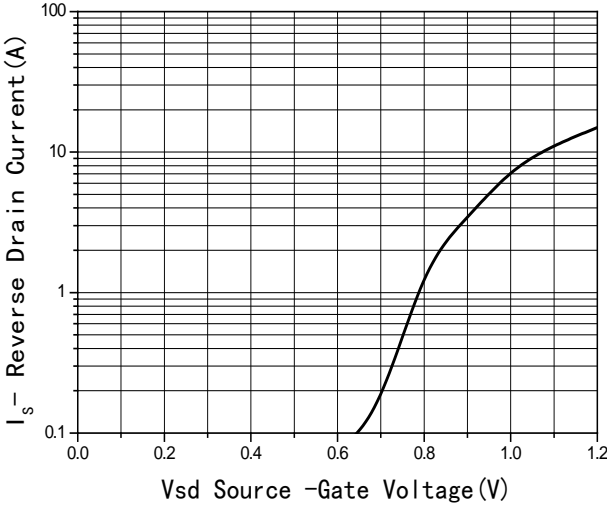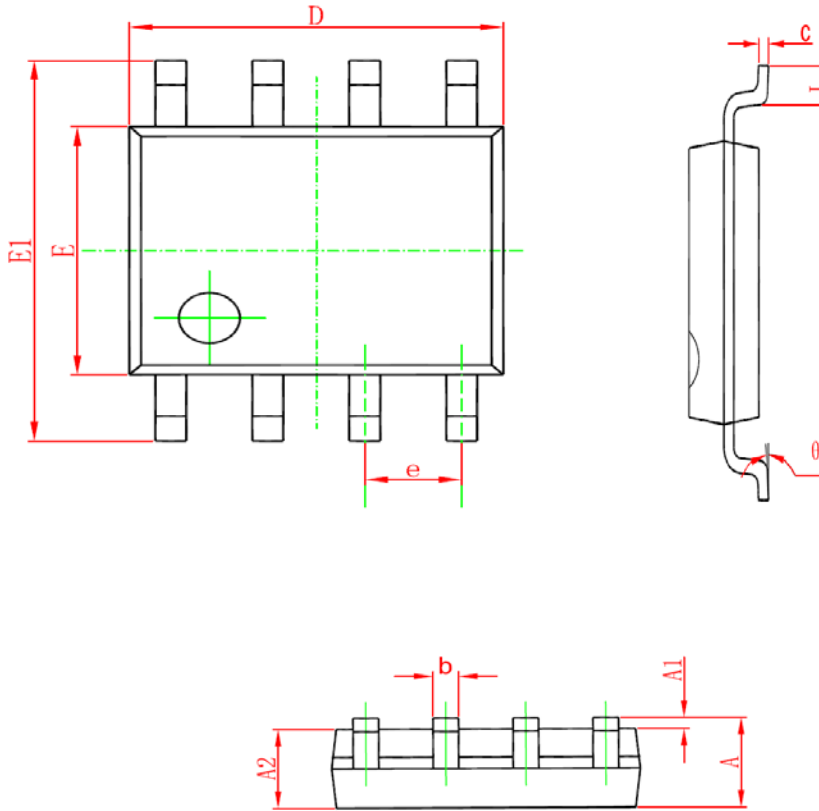

Fig6 Gate Charge

Fig7 Power De-rating

**Fig8 Source-Drain Diode Forward**

Package Information

● **SOP-8**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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Recommended Minimum Pads

- **SOP-8**
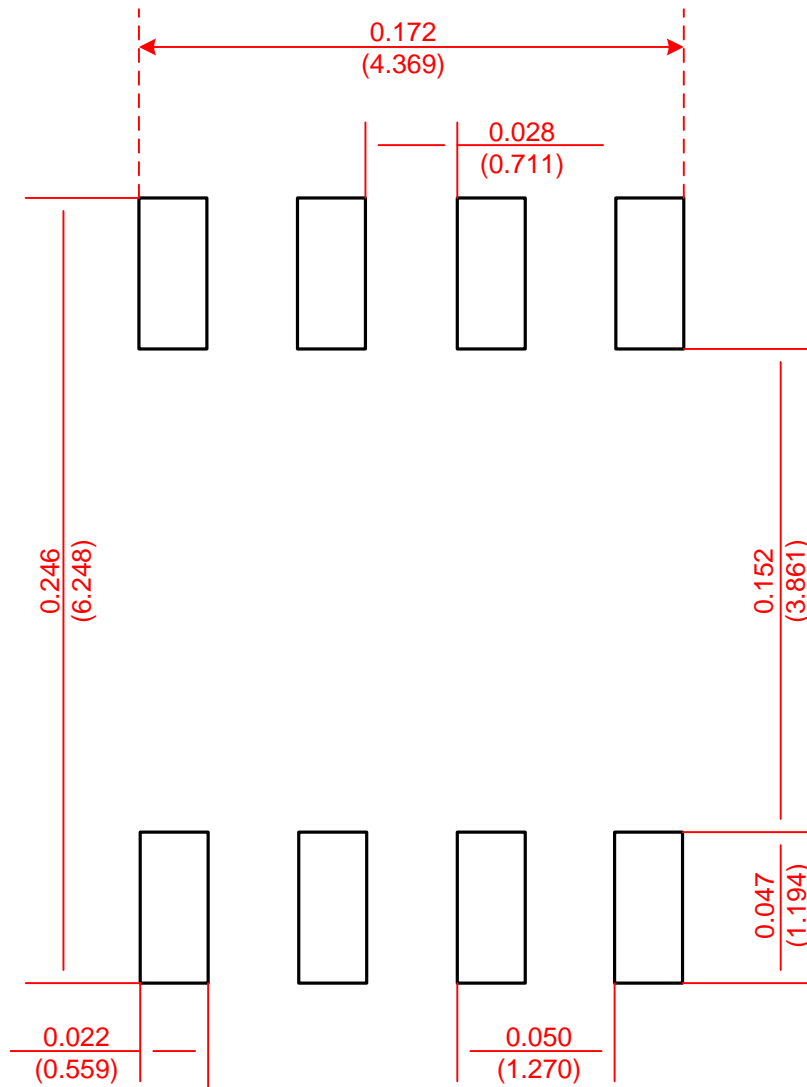
Recommended Minimum Pads
Dimensions in Inches/(mm)