

### 40V Dual N-Channel Enhancement Mode MOSFET

#### Description

The PECN4890D6 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  with low gate charge.

This device is suitable for high side switch in SMPS and general purpose applications.

#### General Features

- ◆  $V_{DS}=40V, I_D=35A$   
 $R_{DS(ON)}=6.3m\Omega$  (typical) @  $V_{GS}=10V$   
 $R_{DS(ON)}=8.5m\Omega$  (typical) @  $V_{GS}=4.5V$
- ◆ Excellent gate charge x  $R_{DS(ON)}$  product(FOM)
- ◆ Very low on-resistance  $R_{DS(ON)}$
- ◆ 150 °C operating temperature
- ◆ Pb-free lead plating
- ◆ 100% UIS tested

#### Application

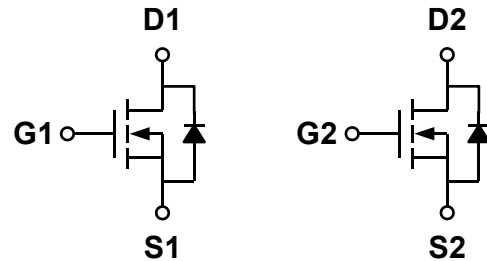
- ◆ DC/DC Converter
- ◆ Ideal for high-frequency switching and synchronous rectification

#### Package

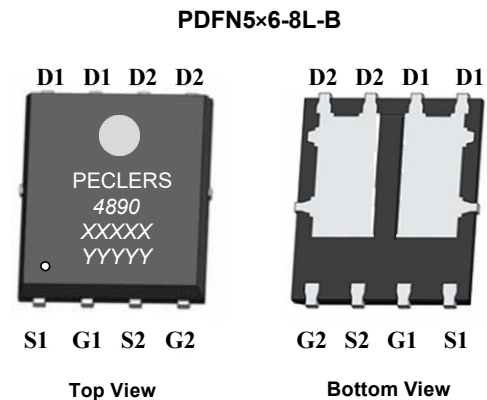
- ◆ PDFN5\*6-8L-B

*100% UIS TESTED!*  
*100%  $\Delta V_{ds}$  TESTED!*

#### Schematic diagram



#### Marking and pin assignment



Note:  
 XXXX is the date code.  
 YYYYY is the Quality Code



#### Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN4890D6	-55°C to +150°C	PDFN5*6-8L-B	5000

#### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit	
Drain-source voltage	$V_{DS}$	40	V	
Gate-source voltage	$V_{GS}$	±20	V	
Drain Current-Continuous (Silicon Limited)	$I_D$	$T_A=25^\circ C$	35	A
		$T_A=75^\circ C$	28	
Pulsed Drain Current (Package Limited)	$I_{DM}$	140	A	
Single pulse avalanche energy (L=0.1mH)	$E_{AS}$	80	mJ	
Maximum power dissipation	$P_D$	$T_A=25^\circ C$	31	W
		$T_A=75^\circ C$	16	

Operating junction Temperature range	T <sub>j</sub>	-55—150	°C
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### Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	40	-	-	V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V	-	-	1	μA
		T <sub>J</sub> = 85°C	-	-	5	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.5	2.3	V
Drain-source on-state resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A	-	6.3	7.5	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A	-	8.5	10	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 12A	-	60	-	S
<b>Diode Characteristics</b>						
Diode Forward Voltage	V <sub>SD</sub>	I <sub>SD</sub> = 1A, V <sub>GS</sub> = 0V	-	0.82	1.1	V
Diode Continuous Forward Current	I <sub>S</sub>		-	-	2.5	A
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 12A, dI/dt = 100A/μs	-	30	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>		-	19	-	nC
<b>Dynamic Characteristics</b>						
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1MHz	-	3.5	-	Ω
Input capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 20V f = 1.0MHz	-	1500	-	pF
Output capacitance	C <sub>OSS</sub>		-	215	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	135	-	
Turn-on delay time	t <sub>D(ON)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, R <sub>L</sub> = 2Ω, R <sub>G</sub> = 3Ω	-	6.4	-	ns
Turn-on Rise time	t <sub>r</sub>		-	17.2	-	
Turn-off delay time	t <sub>D(OFF)</sub>		-	29.6	-	
Turn-off Fall time	t <sub>f</sub>		-	16.8	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, I <sub>D</sub> = 12A	-	27.2	-	nC
Gate-source charge	Q <sub>gs</sub>		-	4.5	-	
Gate-drain charge	Q <sub>gd</sub>		-	6.4	-	

### Thermal Characteristics

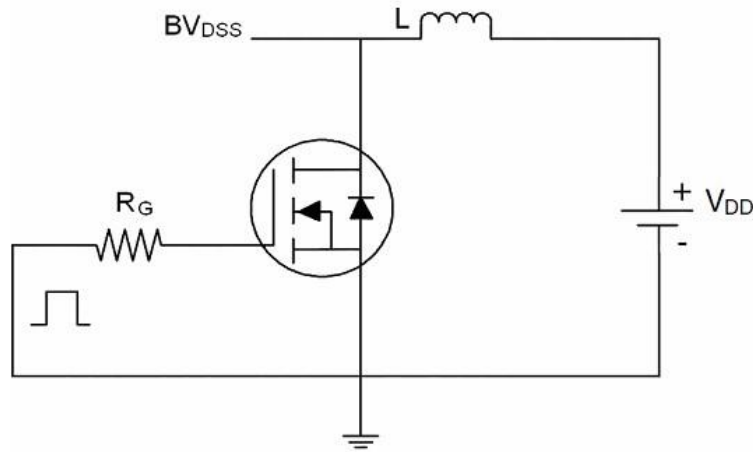
Parameter	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient <sup>A</sup>	≤ 10s	R <sub>θJA</sub>	12	°C/W
Maximum Junction-to-Ambient <sup>A</sup>	Steady-State		33	
Maximum Junction-to-Lead <sup>B</sup>	Steady-State	R <sub>θJC</sub>	2.4	2.9

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> = 25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

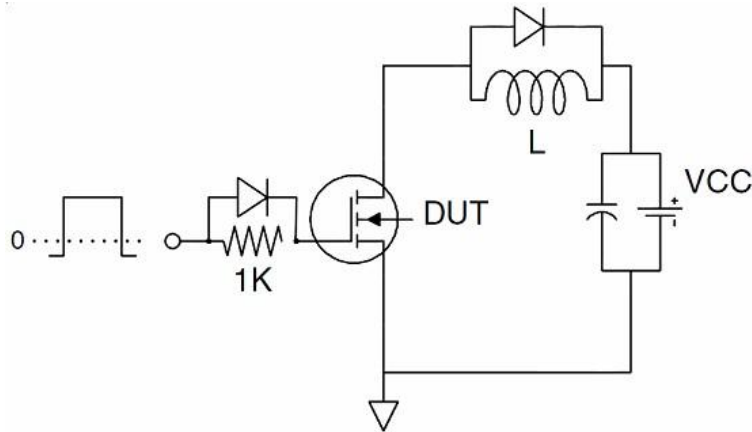
B: The  $R_{qJA}$  is the sum of the thermal impedance from junction to lead  $R_{qJL}$  and lead to ambient.

### Test Circuit:

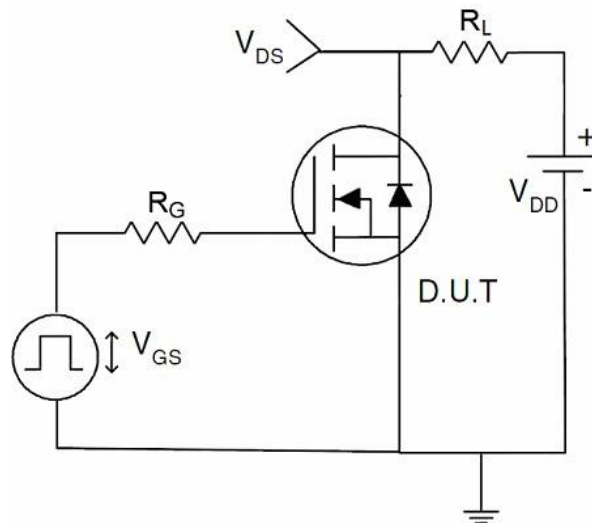
(1)、EAS Test Circuit



(2)、Gate Charge Test Circuit

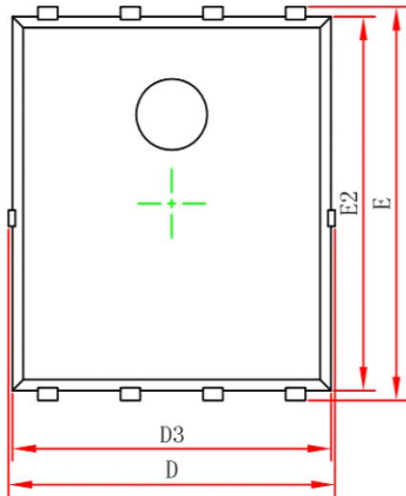


(3)、Switch Time Test Circuit

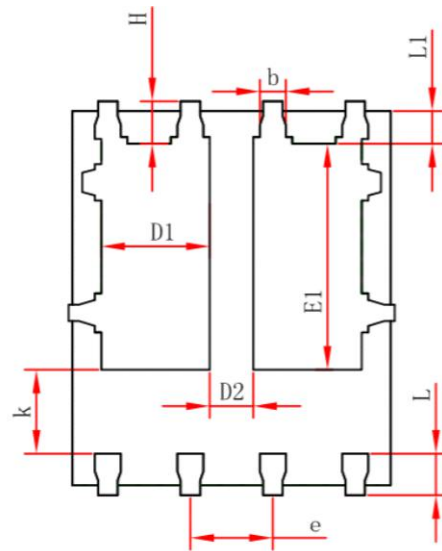


### Package Information

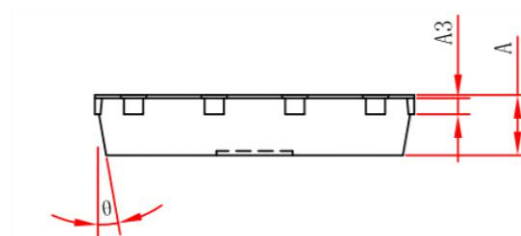
- PDFN5\*6-8L-B



**Top View**



**Bottom View**



**Side View**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°