40V Dual N-Channel Enhancement Mode MOSFET

Description

The PECN6884D6 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge.

This device is suitable for high side switch in SMPS and general purpose applications.

General Features

- V_{DS} =40V,I_D =26A
  $R_{DS(ON)}$=12.5mΩ (typical) @ V_{GS}=10V
  $R_{DS(ON)}$=16.0mΩ (typical) @ V_{GS}=4.5V
- Excellent gate charge x $R_{DS(ON)}$ product(FOM)
- Very low on-resistance $R_{DS(ON)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

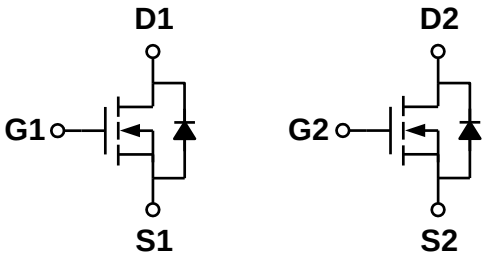
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

Package

- PDFN5*6-8L-B

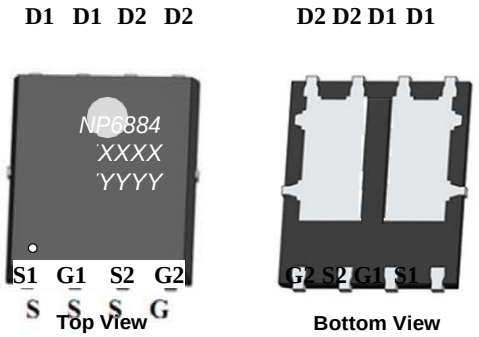
100% UIS TESTED!
100% ΔVds TESTED!

Schematic diagram



Marking and pin assignment

PDFN5×6-8L-B



Note：

XXXX is the date code ,

YYYY is the wafer lot number.

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN6884D6-G	-55°C to +150°C	PDFN5*6-8L-B	5000

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	±20	V
Drain Current-Continuous (Silicon Limited)	T_A=25°C	I_D	26	A
	T_A=75°C		18	
Pulsed Drain Current (Package Limited)		I_{DM}	104	A
Single pulse avalanche energy		E_{AS}	50	mJ
Maximum power dissipation	T_A=25°C	P_D	31	W
	T_A=75°C		16	

Operating junction Temperature range	Tj	-55—150	℃

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	40	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
Gate-body leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	1.4	2.0	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=26A	-	12.5	15	mΩ
		V_{GS}=4.5V, I_D=15A	-	16.0	19	
Forward transconductance	g_{fs}	V_{DS}=5V, I_D=10A	-	50	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	V_{DS}=20V ,V_{GS}=0V f=1.0MHz	-	1500	-	pF
Output capacitance	C_{OSS}		-	215	-	
Reverse transfer capacitance	C_{RSS}		-	135	-	
Gate resistance	Rg	V_{GS}=0V, V_{DS}=0V, f=1.0MHz	-	3.5	5	Ω
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	V_{DS}=20V V_{GS}=10V R_L=1.5Ω R_{GEN}=3Ω	-	6.4	-	ns
Rise time	tr		-	17.2	-	
Turn-off delay time	$t_{D(OFF)}$		-	29	-	
Fall time	tf		-	16	-	
Total gate charge	Q_g	V_{DS}=20V,I_D=10A V_{GS}=10V	-	27	-	nC
Gate-source charge	Q_{gs}		-	4.5	-	
Gate-drain charge	Q_{gd}		-	6.4	-	

Thermal Characteristics

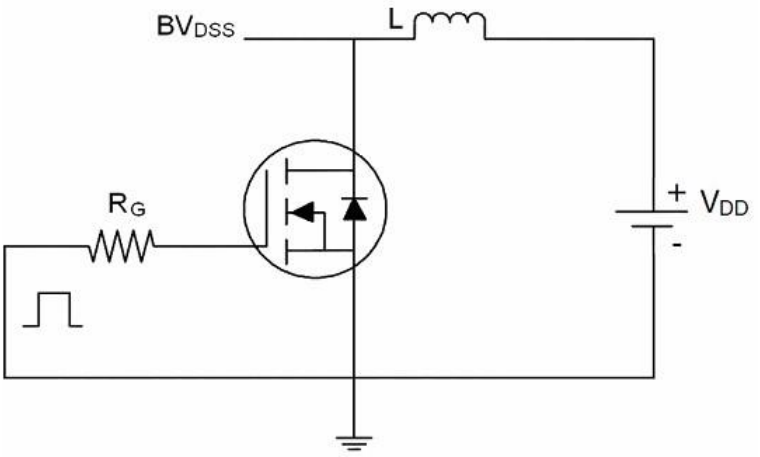
Parameter		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient[A]	≤ 10s	$R_{\theta JA}$	12	20	℃/W
Maximum Junction-to-Ambient[A]	Steady-State		33	50	
Maximum Junction-to-Lead[B]	Steady-State	$R_{\theta JC}$	2.4	2.9	

A:The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

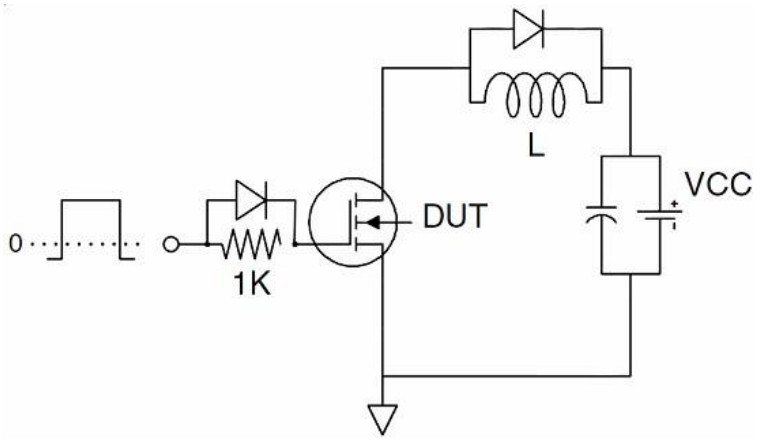
B: The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JC}$ and lead to ambient.

Test Circuit：

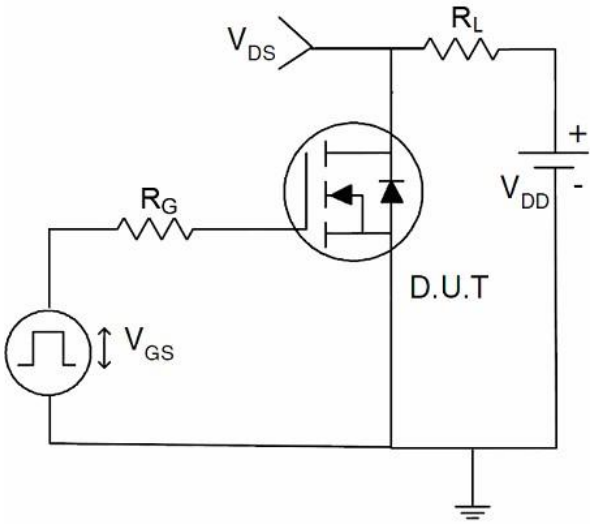
1、EAS Test Circuit



2、Gate Charge Test Circuit

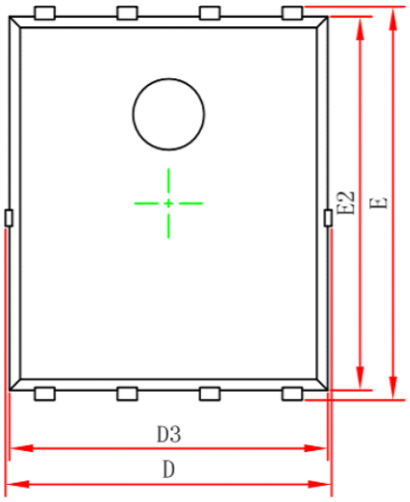


3、Switch Time Test Circuit

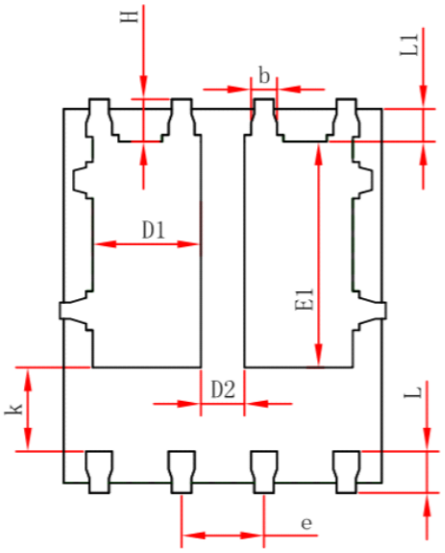


Package Information

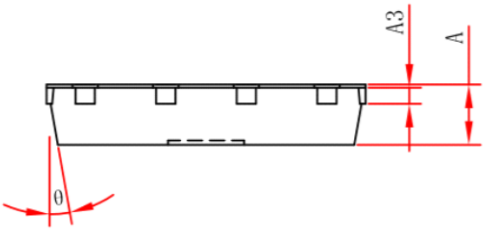
- **PDFN5*6-8L-B**



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°